Docket No.: 42390.P8934

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:
Steven Tu, et al.

Application No. 09/746,487

Filed: December 22, 2000

For: METHOD AND APPARATUS FOR SHARED RESOURCE MANAGEMENT IN A MULTIPROCESSING SYSTEM

Examiner: A. Patel

Art Unit: 2154

CERTIFICATE OF TRANSMISSION

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Date Lawrence M. Mennemeier

APPELLANT'S BRIEF UNDER 37 CFR § 41.37 IN SUPPORT OF APPELLANT'S APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Mail Stop Appeal Brief-Patents
Commissioner of Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant hereby submits this Brief in support of an appeal from a final decision of the Examiner, in the above-referenced case. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interference for allowance of the above-referenced patent application.

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I. Real Party in Interest

The real party in interest in the present appeal is Intel Corporation of Santa Clara, California, the assignee of the present application.

II. Related Appeals and Interferences

There are no related appeals or interferences to appellant's knowledge that would have a bearing on any decision of the Board of Patent Appeals and Interferences.

III. Status of the Claims (independent claims shown in bold)

Claims 1-7 and 8-13 are canceled.

Claims **14**-16, **17**-23, **24**-27 and **28**-30 stand rejected under 35 USC § 103(a) as allegedly being unpatentable over US Pat. No. 5,872,980 (Derrick) in view of US Pat. No. 6,148,395 (Dao).

Final rejection of claims **14**-16, **17**-23, **24**-27 and **28**-30 is being appealed.

IV. Status of Amendments

An amendment and response to a first Office Action mailed 1/5/2004 was submitted by appellant on 4/5/2004 and was entered. A Final Office Action was mailed on 6/10/2004. An RCE and an amendment were submitted by appellant on 9/7/2004 and were entered. Another Office Action was mailed 11/3/2004. Appellant responded by submitting an official response on 5/3/2005, which was entered. A Final Office Action was mailed on 7/11/2005. An amendment after final was submitted by appellant on 12/31/2005, but was not entered. A Notice of Appeal was transmitted on 1/11/2005, and an appeal ensued. An Advisory Action Before the Filing of and Appeal Brief was mailed 2/6/2006. Another amendment is being submitted, under 37 CFR § 41.33 and concurrent with the present appeal brief.

Accordingly, the claims stand as of the concurrently submitted amendment of 3/13/2006, and are reproduced in clean form in the Claims Appendix.

V. Summary of Claimed Subject Matter

Appellant's disclosure describes methods and apparatus for efficient low level management of shared resources in a multiprocessing system. Access to shared resources is provided by a semaphore control mechanism. The semaphore control mechanism provides for a high degree of programmable firmware reuse requiring relatively few modifications in comparison to a processor that does not share resources.

According to one embodiment, a resource scheduling device provides access to a set of resources, shared resources having semaphores. A semaphore checker receives one or more semaphore modification requests from a logical plurality of processors and identifies the ownership state of a semaphore. The semaphore checker arbitrates the semaphore modification requests and allows a particular modification request to succeed if the identified ownership state corresponds to the requesting processor or if the ownership state corresponds to no ownership.

According to an alternative embodiment, there is a register to access a shared resource and a semaphore corresponding to that shared resource. Each of the semaphore modification requests identifies a corresponding requesting processing device. A semaphore checker coupled to the semaphore allows access to the shared resource through the register.

Claim 24 sets forth an apparatus comprising: a register[1] to access a shared resource of a set of resources[2]; a semaphore corresponding to the shared resource; and a semaphore

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[1] "In one embodiment, access to resource 412 or to resource 413 is provided by a hardware level abstraction 414 through a corresponding mode specific register (MSR)." **(Fig. 4, p. 5, lines 10-12)** "Similarly access to shared resource 533 is provided through hardware level abstraction 514 by PLA firmware 511 performing a write operation to corresponding MSR 535." **(Fig. 5, p. 5, lines 20-22)**

[2] "Resource 412 and resource 413 represent exclusive or shared resources such as cache resources, busses or other data transmission resources, parity checking functionality resources, protocol resources, arithmetic unit resources, register resources or any other resources accessed through the hardware level abstraction 414." **(Fig. 4, p. 5, lines 6-10)** "Figure 5 illustrates one embodiment of a multiprocessor 501 comprising a processor 510 that has access to exclusive resources 512 and shared resource 533." **(Fig. 5, p. 5, lines 16-18)**

checker coupled to the semaphore[3] to allow access to the shared resource through the register.

Claim 25 sets forth the apparatus of Claim 24 wherein the semaphore checker is further to: receive one or more semaphore modification requests from one or more of a logical plurality of processing devices, identify an ownership state of the semaphore[4], arbitrate the one or more semaphore modification requests and identify a first modification request from a first requesting device of the one or more of the logical plurality of processing devices[5] to succeed if the identified ownership state corresponds to the first requesting device; and allow the first modification request to succeed if the identified ownership state corresponds to no ownership[6].

Claim 28 sets forth an apparatus comprising: a register[1] to access a shared resource of a set of resources[2]; a semaphore corresponding to the shared resource; and a semaphore checker coupled to the semaphore[3] to allow access to the shared resource through the register, the semaphore checker further to: receive one or more semaphore modification requests from one or more of a logical plurality of processing devices, wherein each of the one or more semaphore modification requests received identify a corresponding requesting device of the one or more of the logical plurality of processing devices, identify an ownership state of the semaphore[4], arbitrate the one or more semaphore modification

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[3] "In one embodiment of a semaphore control mechanism, semaphore MSR 532 and semaphore checker 531 provide mutually exclusive access to shared resource 533 and corresponding MSR 535." **(Fig. 5, p. 5, lines 22-24)**

[4] "Then, in processing block 627, a modification request is made to have the processor identification number in ID written to the semaphore MSR at address SADDR. Afterwards, in processing block 628, the semaphore MSR at address SADDR is tested to see if it contains the same processor identification number in ID." **(Fig. 6b, p. 7, lines 14-18)**

[5] "Multiprocessor 301 also includes first logical machine 311 having exclusive access to L1 cache 312 and a second logical machine 321 having exclusive access to L1 cache 322. Both logical machine 311 and logical machine 321 have shared access to L2 cache 333, and data transmission resource 334." **(Fig. 3, p. 4, line 13-17)** "Semaphore checker 531 arbitrates modification requests to semaphore MSR 532, identifying a single request from one or more semaphore modification requests received, the identified modification request including a processor identification number." **(Fig. 5, p. 5, line 25 through p. 6, line 2)**

[6] "Semaphore checker 531 allows the identified modification request to succeed if the ownership state of semaphore MSR 532 corresponds to the processor identification number (in which case the processor is releasing semaphore MSR 532) or if no processor presently has ownership of semaphore MSR 532." **(Fig. 5, p. 6, lines 2-6)**

requests and identify a first modification request from a first requesting device of the one or more of the logical plurality of processing devices[5] to succeed if the identified ownership state corresponds to the first requesting device; and allow the first modification request to succeed if the identified ownership state corresponds to no ownership[6].

Claim 17 sets forth a multiprocessor comprising: a logical plurality of processors[5]; a resource scheduling device[7] coupled to one or more of the logical plurality of processors to provide access to a set of resources[2]; a shared resource of the set of resources having a semaphore; a semaphore checker coupled to the resource scheduling device and to the semaphore[3] to: receive one or more semaphore modification requests from the one or more of the logical plurality of processors, identify an ownership state of the semaphore, arbitrate the one or more semaphore modification requests and identify a first modification request from a first requesting processor of the one or more of the logical plurality of processors[5], allow the first modification request to succeed if the identified ownership state corresponds to the first requesting processor; and allow the first modification request to succeed if the identified ownership state corresponds to no ownership[6].

Claim 14 sets forth a multiprocessor system comprising: means for receiving one or more semaphore modification requests from one or more requesting devices[3,5,7]; means for identifying an ownership state of a semaphore corresponding to the one or more semaphore modification requests[3,4]; means for arbitrating to identify a first modification request of the one or more semaphore modification requests, the first modification request from a first requesting device[5]; means for granting the first modification request if the identified

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[7] "Figure 6a illustrates a diagram of one embodiment of a process for accessing resources using an MSR of a hardware level abstraction. The process is performed by processing blocks that may comprise software or firmware operation codes executable by general purpose machines or by special purpose machines or by a combination of both." **(Fig. 6a, p. 6, lines 19-23)** "Through use of a semaphore control mechanism as disclosed above, shared access to resources may be provided with relatively few modifications to the PLA firmware that does not support resource sharing. Figure 6b illustrates a diagram of one embodiment of a process for accessing shared resources using a semaphore control mechanism. The starting point to the PAL process to modify a shared MSR is at processing block 620 and processing proceeds to processing block 625." **(Fig. 6b, p. 7, lines 5-11)**

ownership state corresponds to the first requesting device[4,6]; and means for granting the first modification request if the identified ownership state corresponds to no owner[6].

VI. Grounds of Rejection to be Reviewed on Appeal

A. Claims **14**-16, **17**-23, **24**-27 and **28**-30 stand rejected under 35 USC § 103(a) as allegedly being unpatentable over US Pat. No. 5,872,980 (Derrick) in view of US Pat. No. 6,148,395 (Dao).

VII. Argument

A. 35 U.S.C. § 103(a) REJECTIONS

Claims **14**-16, **17**-23, **24**-27 and **28**-30 stand rejected under 35 USC § 103(a) as allegedly being unpatentable over US Pat. No. 5,872,980 (Derrick) in view of US Pat. No. 6,148,395 (Dao).

1. Claims **17**-23, 25-27 and **28**-30 Are Not Obvious.

First, in determining the scope and content of the cited references with regard to the instant claims at issue, appellant respectfully submits that Derrick is directed to a spin buffer to assure data integrity in shared resources in a computer system. Concurrent accesses to different semaphores by different devices are allowed. Lock and identification data within the semaphore is cached in the spin buffer so a device requesting access to a shared resource that corresponds to a semaphore that is represented in the spin buffer may determine whether any other device has ownership of the shared resource by accessing the data within the spin buffer, rather than reading from the semaphore (Abstract).

When a device in the computer system of Derrick needs a shared resource, it initiates a read to establish ownership of that resource (Fig. 2, step 202). While reading for ownership, the device only locks out accesses by other devices to that same semaphore (step 204). This allows other devices to access other semaphores while the requesting device is acquiring ownership of the requested shared resource. The requesting device then checks to see if the shared resource it is requesting is already owned by another device (step 206). If the shared resource is owned by another device, the

requesting device must spin and try to gain ownership of the shared resource at a later time. If the device must spin, it unlocks accesses to the semaphore (step 208) so that other devices may access the semaphore. If the requested shared resource is not owned by another master, the requesting device acquires ownership by setting a lock bit (step 210), which indicates to other devices that the requesting device owns the shared resource (Fig. 2; col. 3, line 55 through col. 4, line 6).

Dao does not disclose or suggest any use of semaphores. Dao is directed to a single-chip multiprocessor having multiple central processing units, or CPUs, that share a floating-point unit. A dispatch unit in the floating-point unit performs arbitration between floating-point instructions if more than one of the CPUs is forwarding instructions to the floating-point unit at the same time. Dedicated register banks, are provided in the floating-point unit to store results for each of the CPUs (Abstract, col. 8, lines 6-7; Figs. 3 and 6, 60_0 and 60_1).

Next, appellant respectfully points out some of the differences between the cited references and the instant claims at issue. Claim 17, for example, sets forth:

> 17. (Previously Presented) A multiprocessor comprising:
> a logical plurality of processors;
> a resource scheduling device coupled to one or more of the logical plurality of processors to provide access to a set of resources;
> a shared resource of the set of resources having a semaphore; and
> a semaphore checker coupled to the resource scheduling device and to the semaphore to:
> receive one or more semaphore modification requests from the one or more of the logical plurality of processors,
> identify an ownership state of the semaphore,
> arbitrate the one or more semaphore modification requests and identify a first modification request from a first requesting processor of the one or more of the logical plurality of processors,
> allow the first modification request to succeed if the identified ownership state corresponds to the first requesting processor and
> allow the first modification request to succeed if the identified ownership state corresponds to no ownership.

Similarly, Claim 25 also sets forth:

> 25. (Previously Presented) The apparatus of Claim 24 wherein the semaphore checker is further to:
> receive one or more semaphore modification requests from one or more of a logical plurality of processing devices,
> identify an ownership state of the semaphore,
> arbitrate the one or more semaphore modification requests and identify a first modification request from a first requesting device of the one or more of the logical plurality of processing devices to succeed if the identified ownership state corresponds to the first requesting device; and
> allow the first modification request to succeed if the identified ownership state corresponds to no ownership.

Additionally, Claim 28 sets forth:

> 28. (Previously Presented) An apparatus comprising:
> a register to access a shared resource of a set of resources;
> a semaphore corresponding to the shared resource; and
> a semaphore checker coupled to the semaphore to allow access to the shared resource through the register, the semaphore checker further to:
> receive one or more semaphore modification requests from one or more of a logical plurality of processing devices, wherein each of the one or more semaphore modification requests received identify a corresponding requesting device of the one or more of the logical plurality of processing devices,
> identify an ownership state of the semaphore,
> arbitrate the one or more semaphore modification requests and identify a first modification request from a first requesting device of the one or more of the logical plurality of processing devices to succeed if the identified ownership state corresponds to the first requesting device; and
> allow the first modification request to succeed if the identified ownership state corresponds to no ownership.

The cited references do not disclose or suggest a semaphore checker to receive the semaphore modification requests, to identify an ownership state of the semaphore and to allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device.

In the Final Office Action of July 1, 2005 (p. 16, line 16 through p. 17, line 1) the Examiner states with regard to Claim 17 that it would have been obvious for one in ordinary skill in the art at the time the invention was made to design a means which causes [a] machine to receive the requests for semaphore modifications, to identify an ownership state of a semaphore corresponding to semaphore modification requests,

arbitrate and allow the modification to succeed as desired, in this case the first modification request to succeed if the identification ownership state corresponds to the first requesting device. To this end, the Examiner does not even suggest that Dao contributes anything at all.

Without modification the bus controller and the spin buffer of Derrick do not check the ownership state and so semaphore access may be granted to a spinning device and denied to the device with ownership (Fig. 2, col. 3, lines 57-67).

The appellant respectfully submits (in accordance with MPEP 2143.01) that, especially when no modification is suggested by any of the references, such modification should not be considered obvious.

Appellant respectfully submits that the Final Office Action (p. 16, lines 5-16) is in error for viewing the prior art bus controller and spin buffer of Derrick in retrospect with the aid of appellant's disclosure to arbitrate semaphore modification requests as set forth in Claims 17, 25 and 28.

Derrick's bus controller (Fig. 4, 402) and/or arbiter (Fig. 5, 506) do not have access to the ownership state of semaphores. Yet the bus controller determines the order for granting requests to shared resources (col. 4, lines 47-50).

With regard to the operation of spin buffer (Fig. 5, 502), Derrick discloses that while reading for ownership (Fig. 2, 202), the device locks out accesses by other devices to that same semaphore (step 204). The requesting device with access then checks to see if the shared resource it is requesting is already owned by another device (step 206). If the shared resource is owned by another device, the requesting device must spin and try to gain ownership of the shared resource at a later time. If the device must spin, it unlocks

accesses to the semaphore (step 208) so that other devices may access the semaphore (Fig. 2; col. 3, line 58 through col. 4, line 3).

Thus one difference between the cited references and the instant claims is that in the instant claims a semaphore checker receiving the semaphore modification requests identifies an ownership state of the semaphore and arbitrates the semaphore modification requests allowing a first modification request to succeed if the ownership state corresponds to the requesting processor or if the ownership state corresponds to no ownership.

Such is not the case with Derrick. In order to guarantee exclusive accesses, Derrick does not change the practice of requiring the requesting device to clear the lock bit even if the semaphore would indicate that the shared resource is not owned (Fig. 3, step 310, col. 4, lines 23-28). If the spin buffer of Derrick receives a request for a semaphore from a requesting device before the lock bit has been cleared by another device, it can not allow the request to succeed even if the ownership state corresponds to the requesting device or corresponds to no ownership. Since the spin buffer of Derrick does not check the ownership state, semaphore access can be granted to a spinning requesting device and denied to the device with ownership (Fig. 2, col. 3, lines 57-67).

Therefore, appellant respectfully submits that without viewing the prior art in retrospect with the aid of appellant's disclosure, no suggestion is provided by Derrick or Dao for doing what appellant has done.

For example, if as suggested in the Final Office Action (p. 16, lines 15-16) Derrick's bus controller and/or arbiter were to grant requests for two processors in a round-robin order, a request from a processor that was the owner of a frequently shared

semaphore would be granted approximately 50% of the time and the requesting processor/owner would have to spin approximately 50% of the time because bus controller and/or arbiter grant requests to the shared resources but do not have access to the ownership state of semaphores in the way that appellant's claimed semaphore checker does. Thus in Derrick's system, satisfying a request from a processor that is the owner of a frequently shared semaphore would require on average at least one and one-half requests in a two-processor system--even if the request is just to relinquish the shared semaphore. In the mean time any other processor that does gain access cannot obtain ownership since the processor that is the owner is spinning while waiting to relinquish the shared semaphore.

On the other hand, the semaphore checker set forth in the instant claims may reduce the average number of requests to just one request for a processor that is the owner of a semaphore. Such reductions are statistically significant.

Further, as described in great detail in the present application (pp. 8-14) multiprocessors that provide shared access to resources may introduce new complexities.

For example, when a requesting processor crashes or fails after gaining access to one of Derrick's semaphores but before unlocking accesses to the semaphore (step 208), even if that requesting processor is not the owner of the semaphore, the problem may be very difficult to detect or to correct. This is because Derrick's bus controller and/or arbiter grant requests to shared resources but do not have access to the ownership state of the semaphore whereas the spin buffer simply locks out access to the semaphore by any other device (Fig. 2, step 204; col. 4, lines 47-50).

On the other hand, when in the claimed multiprocessor an error condition has

arisen that requires corrective action, the semaphore checker as set forth in the instant claims may used effectively with respect to error detection, correction and recovery (Detailed Description, pp. 8-14). Such considerations are of practical significance in the field of microprocessor design.

Accordingly in light of the above arguments, Claims **17**-23, 25-27 and **28**-30 are not obvious in view of the cited references.

2. Claims 14-16 Are Not Obvious.

With regard to Claim **14**, the Final Office Action of July 11, 2006 (p. 13, lines 11-14 and 18) rejects the claim for the same reason as Claim 1 where states (p. 9, lines 11-17) that it would have been obvious for one in ordinary skill in the art at the time the invention was made to design a means which causes [a] machine to receive the requests for semaphore modifications, to identify an ownership state of a semaphore corresponding to semaphore modification requests, arbitrate and allow the modification to succeed as desired, in this case the first modification request to succeed if the identification ownership state corresponds to the first requesting device.

Appellant respectfully submits that the Final Office Action (p. 13, lines 11-14 and 18) is in error for **(a)** failing to construe the claim limitations under 35 U.S.C. 112, paragraph six, to cover the corresponding structure, material or acts described in the specification and equivalents thereof; and is further in error for **(b)** viewing the prior art bus controller and spin buffer of Derrick in retrospect with the aid of the appellant's disclosure to arbitrate semaphore modification requests as set forth in Claim 14.

Claim 14, for example, sets forth:

> 14. (Original) A multiprocessor system comprising:
> means for receiving one or more semaphore modification requests from one or more requesting devices;
> means for identifying an ownership state of a semaphore corresponding to the one or more semaphore modification requests;
> means for arbitrating to identify a first modification request of the one or more semaphore modification requests, the first modification request from a first requesting device;
> means for granting the first modification request if the identified ownership state corresponds to the first requesting device; and
> means for granting the first modification request if the identified ownership state corresponds to no owner.

Appellant submits that the combination of Derrick and Dao should not be considered equivalent under 35 U.S.C. 112, paragraph six, to the subject matter set forth in Claim 14.

The MPEP § 2181 states that:

When making a determination of patentability under 35 U.S.C 102 or 103, past practice was to interpret a "means or step plus function" limitation by giving it the "broadest reasonable interpretation." Under the PTO's long-standing practice this meant interpreting such a limitation as reading on any prior art means or step which performed the function specified in the claim without regard for whether the prior art means or step was equivalent to the corresponding structure, material or acts described in the specification. However, in Donaldson, the Federal Circuit stated:

> Per our holding, the "broadest reasonable interpretation" that an examiner may give means-plus-function language is that statutorily mandated in paragraph six. Accordingly, the PTO may not disregard the structure disclosed in the specification corresponding to such language when rendering a patentability determination.

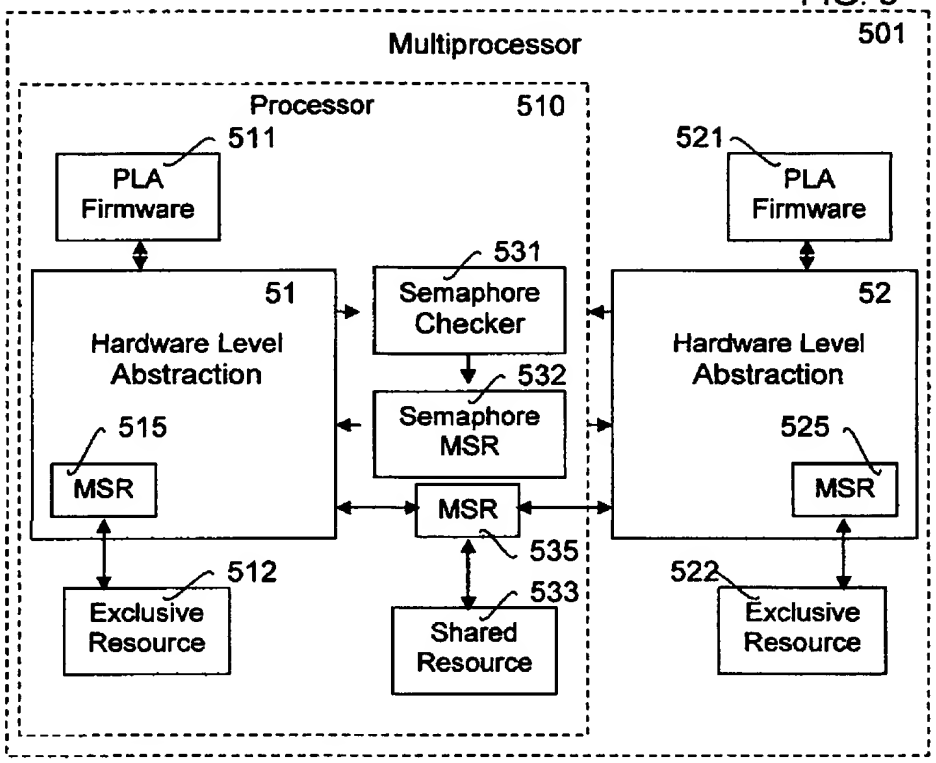
Therefore, appellant submits that Claim 14 should be construed to cover the corresponding structure, material or acts described in the specification and equivalents thereof.

For example, the specification of the present application (Fig. 6b, p. 7, lines 5-11) discloses:

> Through use of a semaphore control mechanism as disclosed above, shared access to resources may be provided with relatively few modifications to the PLA firmware that does not support resource sharing. Figure 6b illustrates a diagram of one embodiment of a process for accessing shared resources using a semaphore control mechanism.

The specification of the present application also shows at Figure 5:

FIG. 5



The specification of the present application (Fig. 5, p. 5, line 16 through p. 6, line 8) also discloses:

> Figure 5 illustrates one embodiment of a multiprocessor 501 comprising a processor 510 that has access to exclusive resources 512 and shared resource 533. Access to exclusive resource 512 is provided through hardware level abstraction 514 by PLA firmware performing a write operation to corresponding MSR 515. Similarly access to shared resource 533 is provided through hardware level abstraction 514 by PLA firmware 511 performing a write operation to corresponding MSR 535. In one embodiment of a semaphore control mechanism, semaphore MSR 532 and semaphore checker 531 provide mutually exclusive access to shared resource 533 and corresponding MSR 535. Semaphore checker 531 arbitrates modification requests to semaphore MSR 532, identifying a single request from one or more semaphore modification requests received, the identified modification request including a processor identification number. Semaphore checker 531 allows the identified modification request to succeed if the ownership state of semaphore MSR 532 corresponds to the processor identification number (in which case the processor is releasing semaphore MSR 532) or if no processor presently has ownership of semaphore MSR 532. Arbitration for new ownership may be decided on a priority basis, or on a round-robin basis, or on any viable combination of chosen arbitration schemes.

Appellant respectfully submits that the spin buffer and/or bus controller of Derrick are not equivalent means for identifying an ownership state of a semaphore corresponding

to one or more semaphore modification requests; equivalent means for arbitrating to identify a first modification request of the one or more semaphore modification requests, the first modification request from a first requesting device; and equivalent means for granting the first modification request if the identified ownership state corresponds to the first requesting device.

For example, it is Derrick's requesting device that checks to see if the shared resource is owned by another device (Fig. 2, steps 204 and 206, col. 3, lines 57-64). The spin buffer of Derrick simply caches semaphores and provides atomic spin-lock access to requesting devices without checking the ownership of the semaphores.

Derrick discloses his invention stating, "According to the present invention, a spin buffer is provided which allows for locking out accesses to each semaphore independently of accesses to other semaphores," (col. 2, lines 61-63).

Access to a semaphore of Derrick needs to be locked and unlocked by the requesting device to guarantee exclusive access and to allow another device to perform a semaphore operation--even to allow a device that currently owns the desired shared resource to relinquish ownership (col. 2, lines 33-37; Fig. 2, step 208, col. 3, line 67 through col. 4, line 2).

On the other hand the claimed means for identifying an ownership state of a semaphore does not cash semaphores or lock them for atomic external access. An absence of the properties of Derrick's spin buffer in the claimed invention is further evidence of nonobviousness. Because the claimed means for identifying an ownership state checks the semaphore rather than the requesting device, it is inherently atomic and provides for more efficiently granting modification request when the identified ownership state

corresponds to a requesting device and when the identified ownership state corresponds to no owner.

Without modification the bus controller and the spin buffer of Derrick do not check the ownership state and so semaphore access may be granted to a spinning device and denied to the device with ownership (Fig. 2, col. 3, lines 57-67).

The appellant respectfully submits (in accordance with MPEP 2143.01) that, especially when no modification is suggested by any of the references, such modification should not be considered obvious.

Therefore, the appellant respectfully submits that the claimed means for identifying an ownership state of a semaphore would not be obvious from the cited references.

Derrick's bus controller (Fig. 4, 402) and/or arbiter (Fig. 5, 506) do not have access to the ownership state of semaphores. Yet the bus controller determines the order for granting requests to shared resources (col. 4, lines 47-50).

With regard to the operation of spin buffer (Fig. 5, 502), Derrick discloses that while reading for ownership (Fig. 2, 202), the device locks out accesses by other devices to that same semaphore (step 204). The requesting device with access then checks to see if the shared resource it is requesting is already owned by another device (step 206). If the shared resource is owned by another device, the requesting device must spin and try to gain ownership of the shared resource at a later time. If the device must spin, it unlocks accesses to the semaphore (step 208) so that other devices may access the semaphore (Fig. 2; col. 3, line 58 through col. 4, line 3).

In order to guarantee exclusive accesses, Derrick does not change the practice of

requiring the requesting device to clear the lock bit even if the semaphore would indicate that the shared resource is not owned (Fig. 3, step 310, col. 4, lines 23-28). If the spin buffer of Derrick receives a request for a semaphore from a requesting device before the lock bit has been cleared by another device, it can not allow the request to succeed even if the ownership state corresponds to the requesting device or corresponds to no ownership. Since the spin buffer of Derrick does not check the ownership state, semaphore access can be granted to a spinning requesting device and denied to the device with ownership (Fig. 2, col. 3, lines 57-67).

Thus one difference between the cited references and the instant claims is that Derrick's spin buffer and bus controller are blind to the ownership state of the semaphore and therefore, are not equivalent means for granting the first modification request if the identified ownership state corresponds to the first requesting device, or equivalent means for granting the first modification request if the identified ownership state corresponds to no owner.

Therefore, appellant respectfully submits that without viewing the prior art in retrospect with the aid of appellant's disclosure, no suggestion is provided by Derrick or Dao for doing what appellant has done.

Accordingly in light of the above arguments, Claims 14-16, are not obvious in view of the cited references.

3. Claim 24 Is Not Obvious.

First, in determining the scope and content of the cited references with regard to the instant claim at issue, appellant respectfully submits that Derrick describes the operation of a spin buffer, which allows for locking out accesses to each semaphore independently of accesses to other semaphores. The spin buffer contains memory locations which indicate whether a requested shared resource is owned by another device. (col. 2, lines 61-66)

Derrick discloses the operation of the spin buffer with regard to Figure 2. When a device needs a shared resource, it initiates a read to establish ownership of that resource. While reading for ownership, the device only locks out accesses by other devices to that same semaphore (step 204). The requesting device then checks to see if the shared resource it is requesting is already owned by another device (step 206). If the shared resource is owned by another device, the device must spin and try to gain ownership of the shared resource at a later time. If the device must spin, it unlocks accesses to the semaphore (step 208) so that other devices may access the semaphore (Fig. 2; col. 3, line 55 through col. 4, line 2).

The Examiner does not suggest that Dao contributes anything to making obvious the subject matter set forth in Claim 24.

The Final Office Action is in error for failing to establish a prima facie case of obviousness since the prior art reference(s) have not been shown to teach or suggest all the claim limitations. Further, the Final Office Action does not even attempt to provide a motivation or suggestion to modify or combine references.

Appellant respectfully points out some of the differences between the cited references and the instant claim at issue. Claim 24, for example, sets forth:

> 24. (Original) An apparatus comprising:
> a register to access a shared resource of a set of resources;
> a semaphore corresponding to the shared resource; and
> a semaphore checker coupled to the semaphore to allow access to the shared resource through the register.

Derrick and Dao do not disclose or suggest a register to access a shared resource of a set of resources and a semaphore checker coupled to a corresponding shared resource semaphore to allow access to the shared resource through the register. The Examiner has not suggested that such limitations are explicitly or inherently described by the cited references or that any combination of the references would make such claim limitations obvious to one of ordinary skill in the art.

Appellant respectfully submits that in the present application, it is disclosed that in one embodiment, access to resource 412 or to resource 413 is provided by a hardware level abstraction 414 through a corresponding mode specific register (MSR) (Fig. 4, p. 5, lines 10-12). Similarly access to shared resource 533 is provided through hardware level abstraction 514 by PLA firmware 511 performing a write operation to corresponding MSR 535 (Fig. 5, p. 5, lines 20-22). The combined references have not been shown to teach or suggest such claim limitations.

With regard to Claim **24**, the Final Office Action of July 11, 2005 (p. 19, lines 1-2) states that Derrick's spin buffer (Fig. 6, 502) is a semaphore checker.

Appellant respectfully submits that the spin buffer of Derrick does not check the semaphores but rather caches them and allows a requesting device to check if a shared resource is owned by another device (col. 3, lines 61-65). The spin buffer of Derrick

merely provides atomic spin-lock access by requesting devices to the semaphore. A cache is not a semaphore checker, and a cache does not make obvious the claimed semaphore checker even if that cache is for storing semaphores.

On the other hand the claimed semaphore checker does not cash semaphores or lock them for atomic external access. Rather, it is coupled to a hardware semaphore corresponding to the shared resource. An absence of theses properties of Derrick's spin buffer in the claimed invention is further evidence of nonobviousness. Because the claimed semaphore checker, itself, checks the semaphore rather than the requesting device, it is inherently atomic and more efficient allowing one requesting device access to the shared resource through the register.

Appellant respectfully submits that since the requesting device simply locks out accesses by other devices to the same semaphore, Derrick's spin buffer is not a semaphore checker as asserted by the Examiner and the cited reference provides no discussion or suggestion of a semaphore checker coupled to a semaphore to allow access to a shared resource as claimed.

Accordingly, the appellant respectfully submits that when the references do not teach or suggest all the claim limitations the Final Office Action can not have established a prima facie case of obviousness.

Accordingly in light of the above arguments, Claims **24** is not obvious in view of the cited references.

Conclusion

Appellant submits that all claims now pending are in condition for allowance. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Acct. No. 02-2666.

Respectfully submitted,

Date: 3-13-06

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VIII. Claims Appendix: Claims Allowed and Involved in Appeal (Clean Copy)

1-13. (Canceled)

14. (Original) A multiprocessor system comprising:
means for receiving one or more semaphore modification requests from one or more requesting devices;
means for identifying an ownership state of a semaphore corresponding to the one or more semaphore modification requests;
means for arbitrating to identify a first modification request of the one or more semaphore modification requests, the first modification request from a first requesting device;
means for granting the first modification request if the identified ownership state corresponds to the first requesting device; and
means for granting the first modification request if the identified ownership state corresponds to no owner.

15. (Original) The multiprocessor system recited in Claim 14 further comprising:
means for receiving a semaphore read requests from one of the one or more requesting devices;
means for transmitting the identified ownership state in response to the semaphore read request; and
means for allowing the first requesting device to access a shared resource.

16. (Original) The multiprocessor system recited in Claim 14 wherein the one or more requesting devices are fabricated on a single die.

17. (Previously Presented) A multiprocessor comprising:
a logical plurality of processors;
a resource scheduling device coupled to one or more of the logical plurality of processors to provide access to a set of resources;
a shared resource of the set of resources having a semaphore; and
a semaphore checker coupled to the resource scheduling device and to the semaphore to:
receive one or more semaphore modification requests from the one or more of the logical plurality of processors,
identify an ownership state of the semaphore,
arbitrate the one or more semaphore modification requests and identify a first modification request from a first requesting processor of the one or more of the logical plurality of processors,

allow the first modification request to succeed if the identified ownership state corresponds to the first requesting processor and

allow the first modification request to succeed if the identified ownership state corresponds to no ownership.

18. (Original) The multiprocessor recited in Claim 17 wherein the semaphore checker is further to:

decline a second modification request of the one or more semaphore modification requests.

19. (Original) The multiprocessor recited in Claim 17 wherein the semaphore checker is further to:

receive a semaphore read requests from one of the one or more of the logical plurality of processors;

transmit the identified ownership state in response to the semaphore read request; and

allow the first requesting processor to access a shared resource.

20. (Original) The multiprocessor recited in Claim 17 wherein each of the one or more semaphore modification requests received identify a corresponding requesting processor of the one or more of the logical plurality of processors.

21. (Original) The multiprocessor recited in Claim 17 wherein the multiprocessor is fabricated on a single die.

22. (Original) The multiprocessor recited in Claim 17 wherein arbitration is resolved on a round-robin basis.

23. (Original) The multiprocessor recited in Claim 17 wherein arbitration is resolved on a priority basis.

24. (Original) An apparatus comprising:

a register to access a shared resource of a set of resources;

a semaphore corresponding to the shared resource; and

a semaphore checker coupled to the semaphore to allow access to the shared resource through the register.

25. (Previously Presented) The apparatus of Claim 24 wherein the semaphore checker is further to:

receive one or more semaphore modification requests from one or more of a logical plurality of processing devices,

identify an ownership state of the semaphore,

arbitrate the one or more semaphore modification requests and identify a first modification request from a first requesting device of the one or more of the logical plurality of processing devices to succeed if the identified ownership state

corresponds to the first requesting device; and

allow the first modification request to succeed if the identified ownership state corresponds to no ownership.

26. (Original) The apparatus of Claim 25 wherein the semaphore checker is further to:

decline a second modification request of the one or more semaphore modification requests.

27. (Original) The apparatus of Claim 25 wherein the semaphore checker is further to:

receive a semaphore read requests from one of the one or more of the logical plurality of processors;

transmit the identified ownership state in response to the semaphore read request; and

allow the first requesting processor to access a shared resource.

28. (Previously Presented) An apparatus comprising:

a register to access a shared resource of a set of resources;

a semaphore corresponding to the shared resource; and

a semaphore checker coupled to the semaphore to allow access to the shared resource through the register, the semaphore checker further to:

receive one or more semaphore modification requests from one or more of a logical plurality of processing devices, wherein each of the one or more semaphore modification requests received identify a corresponding requesting device of the one or more of the logical plurality of processing devices,

identify an ownership state of the semaphore,

arbitrate the one or more semaphore modification requests and identify a first modification request from a first requesting device of the one or more of the logical plurality of processing devices to succeed if the identified ownership state corresponds to the first requesting device; and

allow the first modification request to succeed if the identified ownership state corresponds to no ownership.

29. (Original) The apparatus of Claim 25 wherein the logical plurality of processing devices are integrated on a single die.

30. (Original) The apparatus of Claim 25 wherein arbitration is resolved on a round-robin basis.

IX. Evidence Appendix: Copies of Evidence Relied Upon by Appellant

Exhibit A

i. US Patent 5,872,980 (Derrick).
ii. US Patent 6,148,395 (Dao).

The above cited references were entered in the record by the examiner with the first Office Action mailed on January 5, 2004.

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